6 電子設計自動化研究群

Electronic Design Automation Research Group

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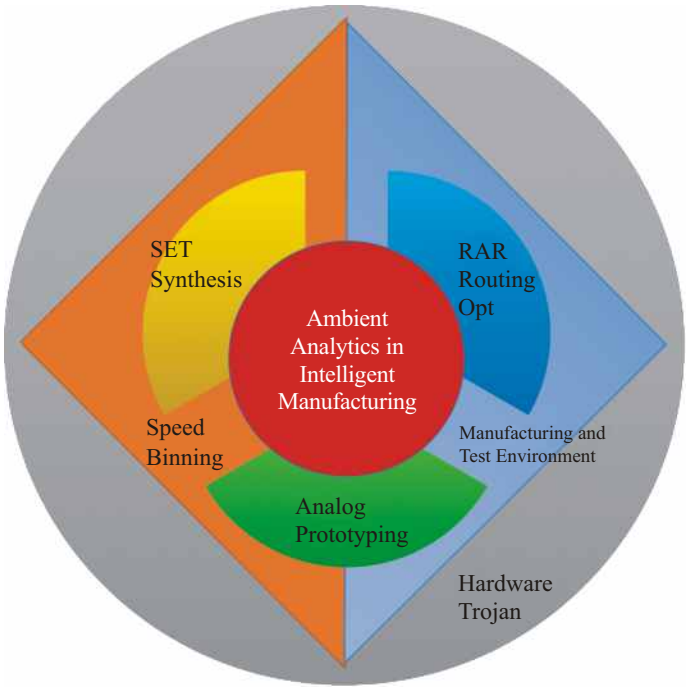
研究方向及特色

針對深次微米時代與物聯網的晶片設計，提出了六大關鍵技術如下：

- 符合次世代晶片上通訊思維之具備幾何考量的系統架構合成技術
- 整合性低耗電管理之技術開發
- 角落錯誤之矽除錯
- 應用計算智慧推理處理後深次微米時代電路設計上的可靠度挑戰
- 考慮可製造化、可靠度與良率的繞線系統
- 晶片層級與系統層級之熱分析技術

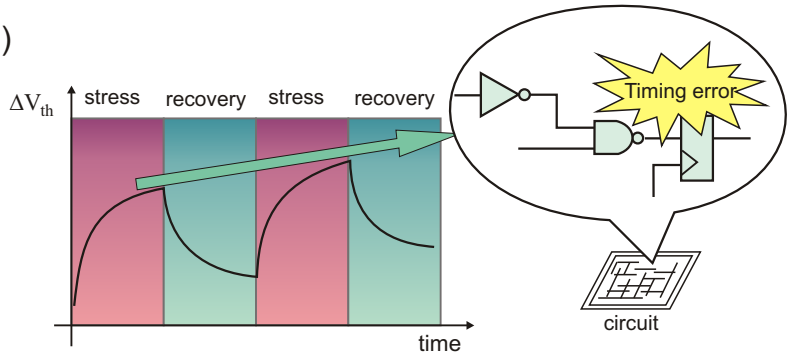
以上技術用以解決目前晶片設計流程中所遇到的急需解決的問題。本研究群提出之相關解決方案，設計出自動化的工具，並可整合進入目前的設計流程，有效的縮短整體的晶片設計時間。涵蓋面包括了：可製造性設計 (Design for Manufacturing, DFM)、可確保良率性設計 (Design for Yield, DFT)、可測試性設計 (Design for Test, DFT) 、除錯化設計 (Design for Debug) 以及低功率設計 (Design for Low-Power)等相關領域。

Ambient analytics from design and silicon data for intelligent VLSI manufacturing

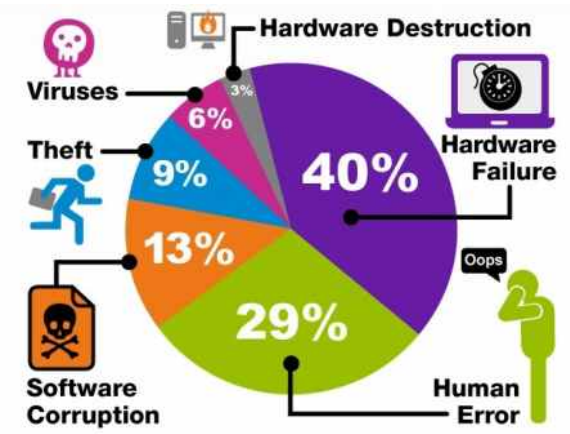


Design for Reliability/Trust

- Reliable (no-less-than-required) computing
  - Low failure/error rate
  - Low performance/timing degradation
  - Long system lifetime

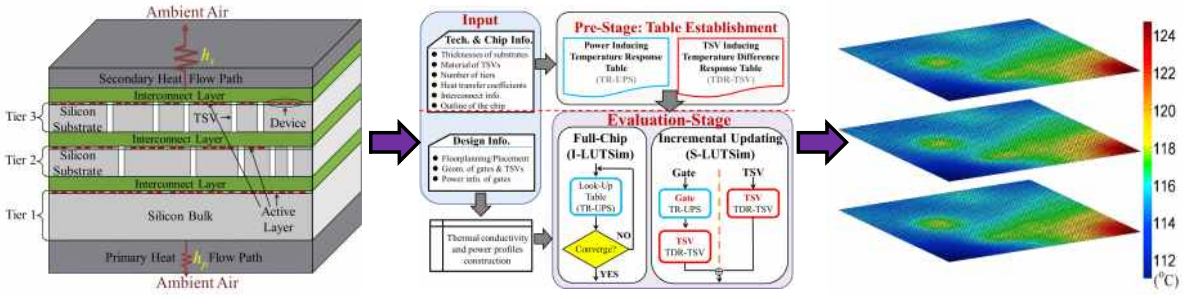


- Trustworthy (no-more-than-required) computing
  - No data leak/theft
  - No hardware sabotage/ destruction
  - High system sustainability



Efficient Thermal Analysis for Chip & System Level Designs

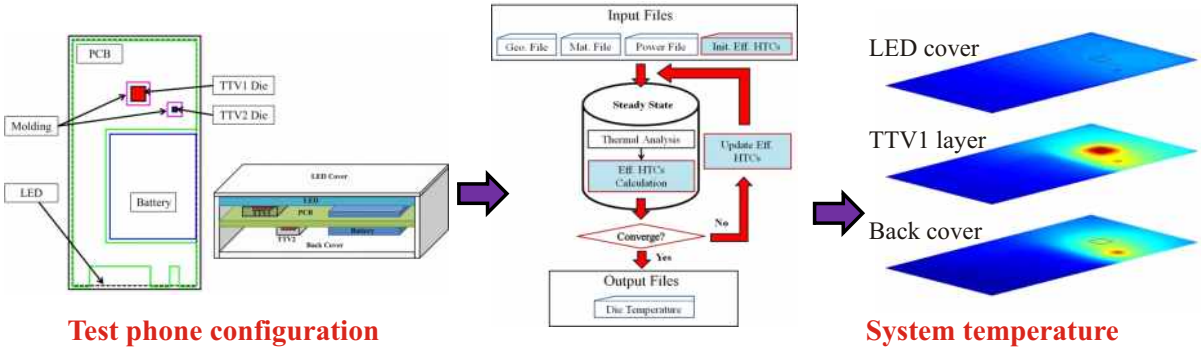
- Chip level thermal simulation



Chip configuration

Chip temperature

- System level thermal simulation

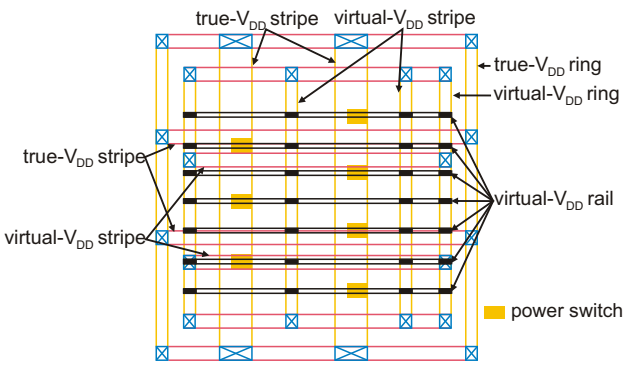


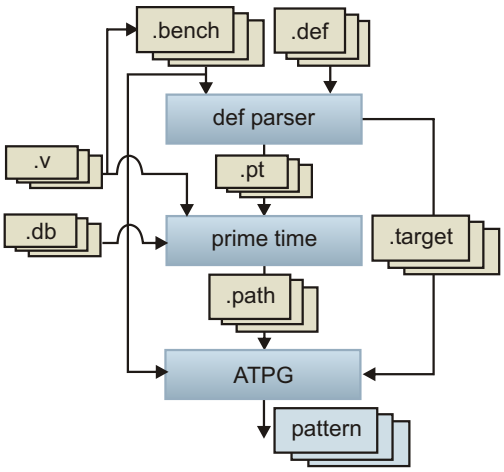
Test phone configuration

System temperature

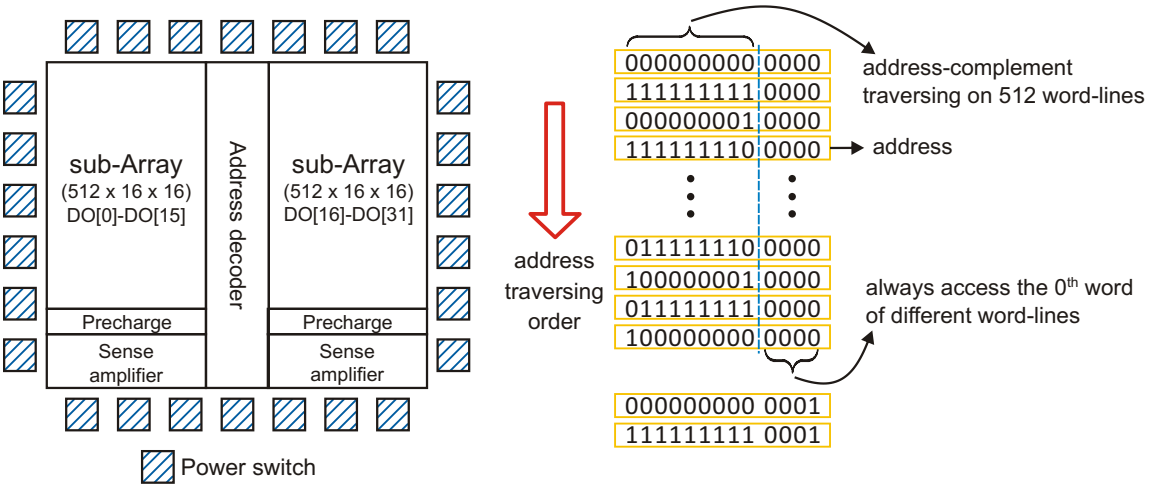
Testing Method for MTCMOS Design

- Testing MTCMOS switches for logic
  - Developed a SAT-based ATPG to generate maximal transitions for target switch and also sensitize a long path





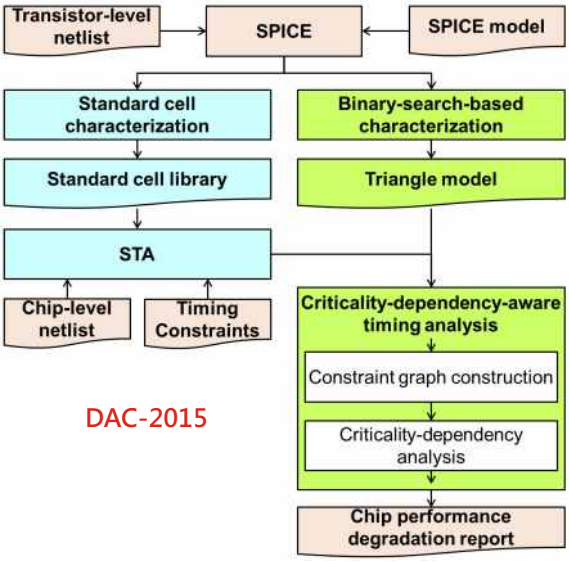
- Testing MTCMOS Switches for SRAMs
  - 1st element: Write each word with alternating opposite data background
  - 2nd element: Read each word in the reverse address traversing as in the 1st element



False Alarms in Timing Analysis

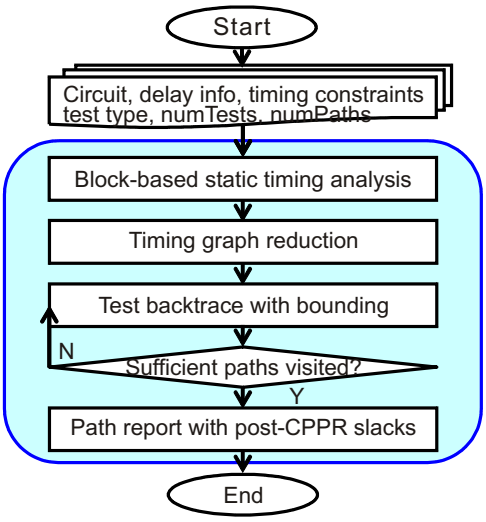
- **False Positive: Criticality-Dependency Effect:** The criticality of the D-pin path affects the timing margin of paths launching from this flip-flop.
- **False Negative: Common path pessimism:** CPPR eliminates artificial pessimism in clock paths to avoid overdesign.

Criticality Dependency Aware Timing Characterization and Analysis Framework



DAC-2015

iTimerC: Fast STA with CPPR Framework



ICCAD-2014, ICCAD-2015
1st place, 2015 ACM TAU Timing Analysis Contest
3rd place, 2014 ACM TAU Timing Analysis Contest