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智慧異質整合研究群

Intelligent Heterogeneous Integration Research Group

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可掃描QRCode進入老師資料簡介



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研究方向及特色

- 數位-類比混合電路在三維環境設計
- 新型奈米材料在TSV之研究
- 微機電元件開發與三維封裝
- 三維積體電路及異質整合之關鍵技術研究
- 2.5D/3D 晶片與封裝及主機板協同設計自動化
- 演算法及模型於三維分層最佳化

未來運作方式及達成目標

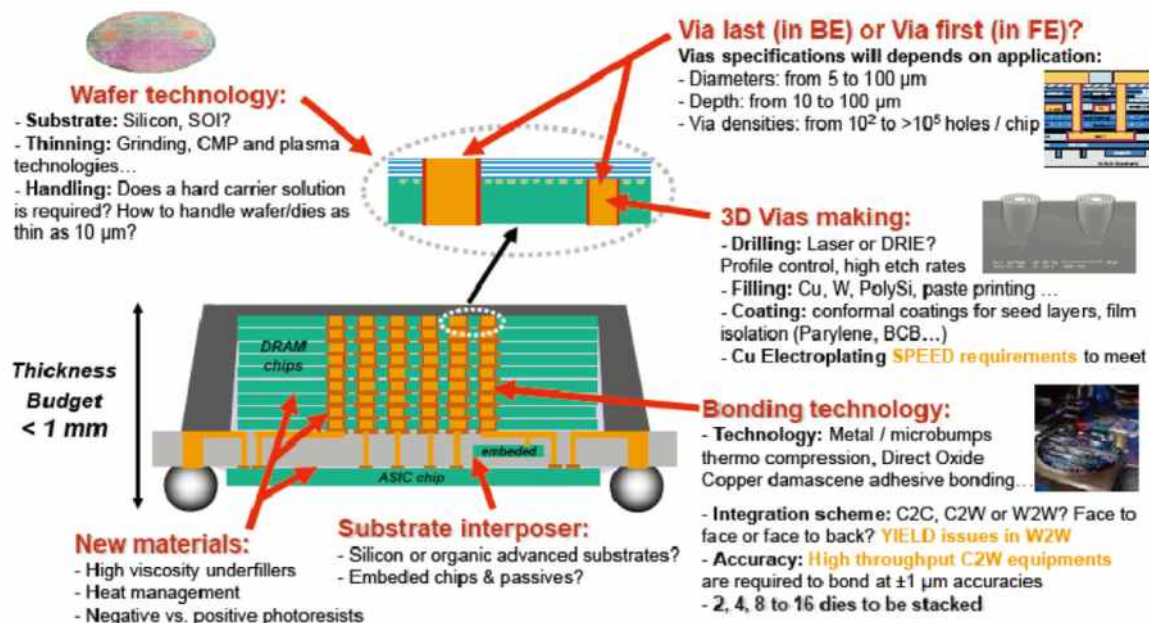
▶ 未來運作方式

本研究群將相互合作，同時包括兩大研究領域。其一為電路設計及自動化在三維積體電路上的研究；其二為三維積體電路製程及應用。各研究實驗室將透過定期開會報告進度、解決研究問題以及分享其成果。

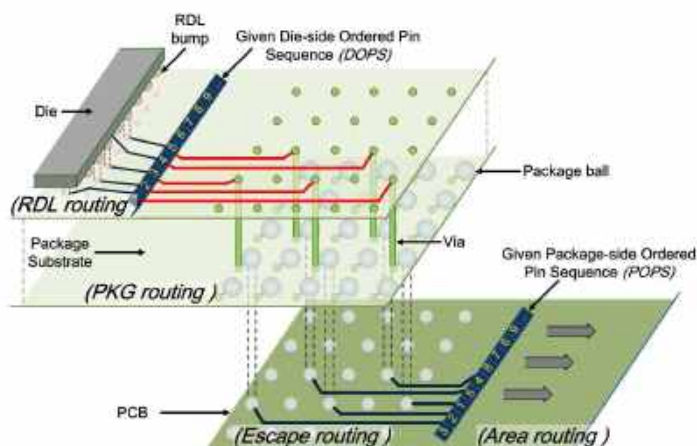
▶ 達成目標

在短期，各實驗室依照研究領域將提出多項整合型研究計畫。再來，積極與國內外產學界合作。最終，培養台灣下世代產業的專業人才也提供台灣電子工業具有深度的研究環境。

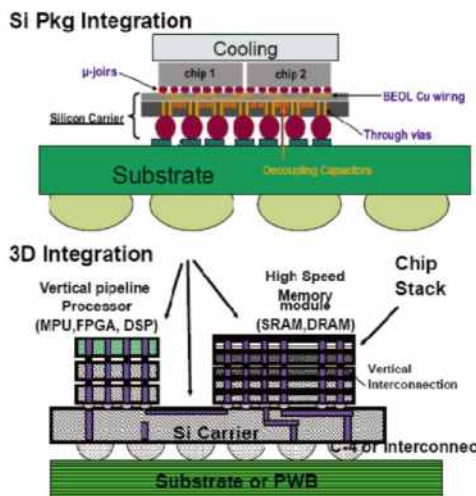
3D ICs: Enabling Technologies



Board- and Chip-Aware Package Wireplanning



3D Integration Challenges & Opportunities

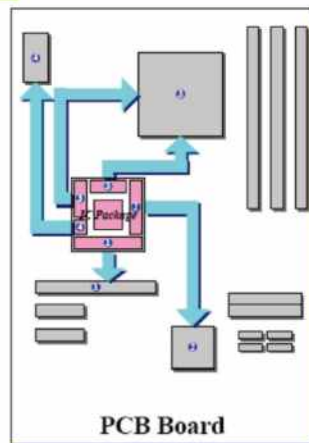


- 3D Technology Challenges:**
1. Through-silicon-vias (TSV)
 2. Fine pitch wiring / high bandwidth
 3. Integrated Decoupling capacitors
 4. High density chip stacking & integration (C2C, C2W, W2W)
 5. Known good die & Die stacks
 6. Advanced cooling
- Opportunities:**
- High bandwidth
 - Low Power
 - Heterogeneous chips
 - Modular Design
 - Modular System Integration
 - System Power Savings
 - System Performance Gain
 - System Miniaturization
 - Time to Market

** 3D SIC 2007 – Knickerbocker et al.

Chip-Package-PCB (System) Co-design

- Chip I/O planning and pin-out designation for flip-chip designs
- Design migration between different package configurations for cost down
- Fast pin-out designation respin for package-board codesign



• Bumpless Interconnecting Technique
Gold-Gold (Au-Au) thermo-compression bonding **without solder ball.**

• 3-8 GHz UWB Tunable Low Noise Amplifier (LNA)

High bump density Design flexibility

Ultra wide band tunable LNA

High-Q micromachined inductor with fine reliability to temperature

Adv.

- 10WBS up to 3-8GHz
- 100 noise and lower power consumption
- 1-50% power saving, > 50% tuning range
- High reliability to temperature

• Integration Result

Reference ground, Microcavities on the carrier, Si Carrier, LNA Chip, Ni/Au bonding pad

• Circuit Simulation Result

• LNA Measurement Result